IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Charles W. Pearce
Serial No.:	09/755,826
Filed:	January 4, 2001
Title:	METHOD OF MANUFACTURING A LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE
Grp./A.U.:	2893
Examiner:	Jack S J Chen
Confirmation No.:	5388

Commissioner for Patents
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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPEAL BRIEF UNDER 37 C.F.R. §41.37

This is an appeal from a Final Rejection dated November 27, 2009, of Claims 1-3, 5-9 and 21. The Appellant submits this Brief with the statutory fee of $540.00 as set forth in 37 C.F.R.§41.20(b)(2), and hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §41.37(c)(1):

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Agere Systems Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-3, 5-9 and 21 are pending in this application and have been rejected under 35 USC §103. Claims 4, 10, 14 and 19 have been canceled, and Claims 11-13, 15-18, 20 and 22-24 have been withdrawn from consideration. Each of the pending claims and are being appealed.

IV. STATUS OF THE AMENDMENTS

The present Application was filed on January 4, 2001. The Appellant filed a first Amendment on January 23, 2003, in response to an Examiner's Action mailed October 24, 2002. The Examiner entered the Amendment and subsequently issued a second Examiner's Action on April 8, 2003. The Appellant then filed a second Amendment on July 8, 2003, in response to the Examiner Action mailed on April 8, 2003. The Examiner entered the second Amendment and subsequently issued a Final Rejection on September 24, 2003. The Appellant then filed a Request for Reconsideration on November 24, 2003. The Examiner indicated that the Request for Reconsideration had overcome the objection to the specification and the rejection under 35 U.S.C. §112, first paragraph, but did not place the Application in condition for allowance. The Appellant then filed a Notice of Appeal on

January 26, 2004, followed by an Appeal Brief on March 22, 2004. In response, the Examiner reopened prosecution in a Rejection dated April 13, 2006. The Appellant then filed a Request for Reconsideration on October 24, 2006 in response thereto. Thereafter, on November 14, 2006, the Examiner issued an advisory action, wherein the Appellant filed a timely Notice of Appeal and Pre-Appeal Brief Document on or about November 27, 2006. The Review Panel, based upon the Pre-Appeal Brief Document, reopened prosecution. The Examiner then issued another non-final Examiner's Action on July 13, 2007. In response thereto, the Appellant filed an Amendment on September 18, 2007. The Examiner entered the Amendment and subsequently issued a Final Rejection on February 27, 2008. In response thereto, the Appellant filed an Amendment on April 23, 2008. Thereafter, on June 2, 2008, the Examiner issued an advisory action, wherein the Appellant filed a timely RCE with preliminary amendment on June 20, 2008. The Examiner then issued an Election Restriction on September 19, 2008, the Appellant responding on October 17, 2008 and January 26, 2009. The Examiner then issued another non-final Examiner's Action on May 29, 2009. In response thereto, the Appellant filed an Amendment on August 31, 2009. The Examiner entered the Amendment and subsequently issued a Final Rejection on November 27, 2009. In response thereto, the Appellant filed a Request for Reconsideration on November 27, 2009. Thereafter, on February 18. 2010, the Examiner issued an advisory action, wherein the Appellant filed a timely Notice of Appeal and Pre-Appeal Brief Document on or about February 26, 2010. A Notice of Panel Decision from Pre-Appeal Brief Review was issued on March 23, 2010, the Notice maintaining the Examiner's rejections. Appellant states that no amendments to the claims were filed subsequent to the final rejection dated November 27, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed, in general, to a semiconductor device and, more specifically, to a method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device. In one embodiment, the method includes forming a lightly-doped source/drain region 310 between first and second isolation structures 215, wherein the lightly-doped source/drain region 310 only includes a first dopant and are formed without the use of a mask layer between the first and second isolation structures. The method further includes creating a gate 410 over the lightly-doped source/drain region 310. As illustrated in FIGUREs 3 & 4 (reproduced here as Illustration 1 & Illustration 2) the lightly-doped source/drain region 310 is formed prior to the formation of the gate 410.

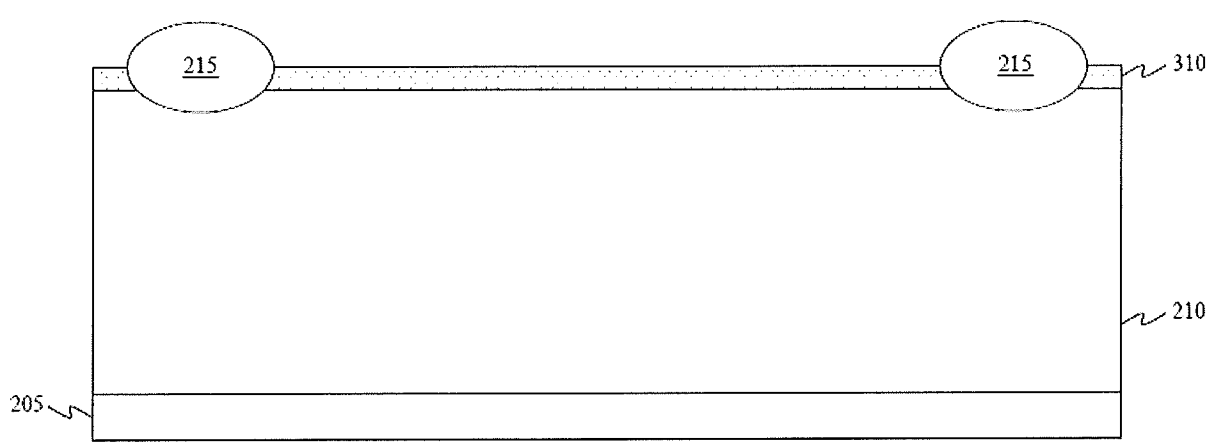

FIGURE 3

Illustration 1

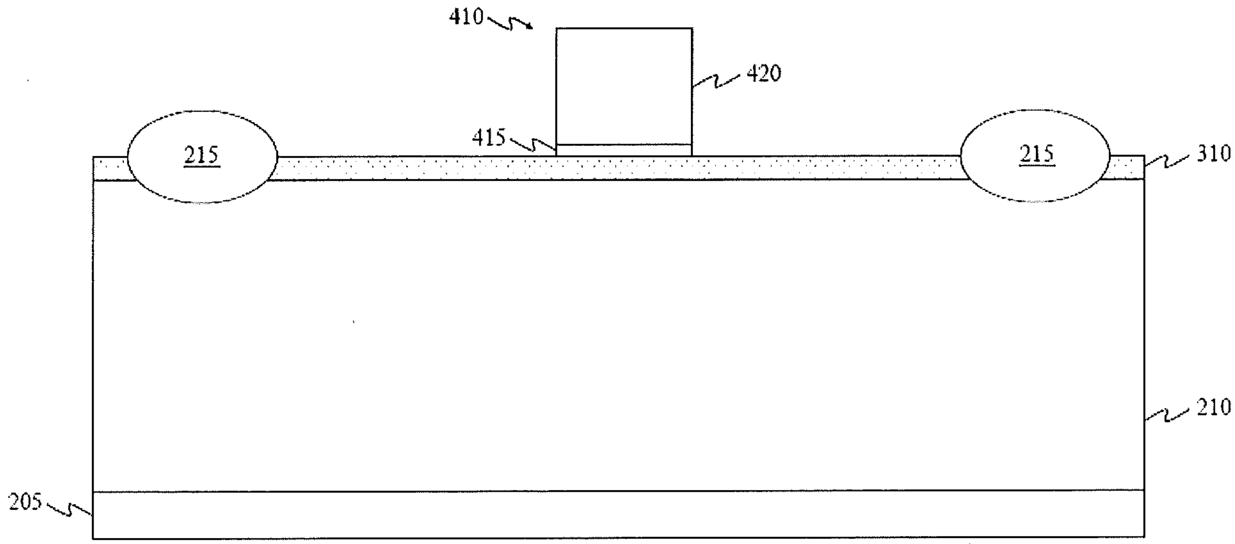

FIGURE 4

Illustration 2

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first issue presented for consideration in this appeal is whether Claims 1-3 and 5-9 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,841,166 to D'Anna *et al.* ("D'Anna"). The second issue presented for consideration in this appeal is whether Claims 1-3 and 21 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 4,918,026 to Kosiak *et al.* ("Kosiak").

VII. APPELLANT'S ARGUMENT

The inventions set forth in independent Claim 1, and its respective dependent claims are patentable under 35 U.S.C. §§103.

<u>Rejection under 35 U.S.C. §103 over D'Anna</u>

The Examiner has rejected Claims 1-3 and 5-9 under 35 U.S.C. §103(a) as being unpatentable over D'Anna. Independent Claim 1 currently includes the element of forming a lightly-doped source/drain region between first and second isolation structures and with only a first dopant and without the use of a mask layer between the first and second isolation structures. D'Anna fails to teach or suggest this element.

D'Anna is directed to a lateral DMOS transistor for RF/microwave applications. (Title). D'Anna teaches that a P+sinker **44** is formed within a P-epi layer **42.** D'Anna then teaches that an N-drift region 46 is formed within the P-epi layer **42** proximate the P+sinker **44.** (See, D'Anna at column 2, lines 54-56). Because of this order of formation, the N-drift region **46** inevitably must to use one or more masks during its formation such that it does not counter dope the P+sinker **44**. D'Anna then teaches that an active area mask is formed to define where the field oxides **52** will be present, and that the field oxides **52** are then grown to a thickness of 0.5 to 3 microns. (See, D'Anna at column 2, lines 59-65). Accordingly, D'Anna teaches first forming its P+sinker **44**, then forming its N-drift region **46** using one or more masks, and only then forming its field oxides **52.** In contrast, Claims 1 and 11 currently require first forming first and second isolation structures and then forming a lightly-doped source/drain region between the first and second isolation structures without the use of a mask. As the Examiner likens the N-drift region **46** of D'Anna to the claimed lightly doped source/drain region, as well as the field oxides **52** of D'Anna to the claimed isolation structures, D'Anna must fail to teach or suggest the element of forming a lightly-doped source/drain region between first and second isolation structures, as well as that the lightly-doped source/drain regions are formed with only a first dopant and without the use of a mask layer.

The Examiner, has only begun to argue that the order of forming the isolation structures with respect to the lightly-doped source/drain region is an obvious design choice over the teachings and suggestions of D'Anna. The Applicant strongly disagrees with this assertion. First, D'Anna goes to great effort and

expense to form its field oxide regions **52** after formation of its doped sinker region **44** and N- drift region **46**. Specifically, D'Anna devotes an entire paragraph (see, Column 2, lines 47-65) to this specific process.

> FIGS. **3A–3D** are side views in section taken along the line **3—3** of FIG. **2** and illustrate steps in fabricating the device of FIG. **2**. Initially, as shown in FIG. **3A** a P+ substrate **40** and P– epitaxial layer **42** are provided as starting material. Alternatively, the substrate and epitaxial layers can be different conductivity types. A deep P+ Sinker Mask and Implant (Boron at 5E15 dose) is performed for source grounding. For a P– or P+ substrate an N– drift region **46** is formed (Arsenic, 5E10–5E12 dose). A thin oxide growth (150 to 1,500 Å) **48** followed by silicon nitride deposition (0.05 to 0.2 micron) **50** are formed. An active area mask is formed by etching the nitride where the field oxide **52** will be present. The doped sinker region **44** is driven in at 1,000°–1,270° C. for 60–800 minutes and the field oxide **52** is grown to a thickness of 0.5 to 3 microns.

Furthermore, D'Anna apparently uses the process of growing the field oxide region **52** to drive in the doped sinker region **44**, or vice versa. Accordingly, it is very important to the process of D'Anna that its field oxide region **52** be formed after implantation of its doped sinker region **44**, and thus after implantation of its N- drift region **46**--so as to drive in the doped sinker region **44**. Accordingly, D'Anna actually teaches away from forming its field oxide region **52** prior to its doped sinker region **44** and N- drift region **46**. Such a teaching away makes the modification suggested by the Examiner non-obvious, and thus merely based upon hindsight. The Board of Appeals is well aware that using hindsight, such as is the case here, is impermissible.

Therefore, D'Anna fails to teach or suggest the invention recited in independent Claim 1 and its dependent claims, when considered as a whole. D'Anna must therefore fail to establish a prima facie case of obviousness with respect to these Claims. It is therefore respectfully submitted that claims 1-3 and 5-9 are not obvious in view of D'Anna.

In view of the foregoing remarks, the cited reference does not support the Examiner's rejection of Claims 1-3 and 5-9 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests that the Board of Appeals remove the rejection of independent Claim 1 and the Claims dependent thereon.

Rejection under 35 U.S.C. §103 over D'Anna

The Examiner has rejected Claims 1-3 and 21 under 35 U.S.C. §103(a) as being unpatentable over Kosiak. As indicated above, independent Claim 1 currently includes the element of forming a lightly-doped source/drain region between first and second isolation structures and with only a first dopant and without the use of a mask layer between the first and second isolation structures. Kosiak fails to teach or suggest this element.

Kosiak is directed to a process for forming a vertical bipolar transistor and high voltage CMOS in a single integrated circuit chip. (Title). Kosiak teaches that lightly doped n-type wells **114**, **214**, and **314** are formed within a substrate **12**. (See, Kosiak at column 4, lines 39-45, and the associated FIG. 2B). Kosiak, by the nature of its manufacturing process, requires that one or more masks **20a, 20b** are needed to form its lightly doped n-type wells **114**, **214**, and **314.** Kosiak then teaches that many other processing steps are performed before forming field oxide regions **50**, **120**, **220**, **320**, and **322** to isolate various different features of the monocrystalline silicon chip **10**. (See, Kosiak at column 5, lines 40-55, and the associated FIG. 2E). Accordingly, Kosiak teaches first forming its lightly doped n-type wells **114**, **214**, and **314** using one or more masks **20a, 20b**, and then forming its field oxide regions **50**, **120**, **220**, **320**, and **322.** This is in direct contrast to that presently claimed within independent Claims 1 and 11, which require forming a lightly-doped source/drain region between first and second isolation structures and with only a first dopant and without the use of a mask layer between the first and second isolation structures. Thus, Kosiak fails to disclose this claimed element.

The Examiner, again only recently, argues that the order of forming the isolation structures with respect to the lightly-doped source/drain region is an obvious design choice over the teachings and suggestions of Kosiak. The Applicant strongly disagrees with this assertion. First, Kosiak goes to great effort and expense to form its field oxide regions **50, 120, 220, 320 and 322** after formation of its lightly doped n-type wells **114, 214**, and **314**. Specifically, Kosiak devotes many paragraphs (see, Column 5, lines 1-45) to this specific process. Furthermore, Kosiak uses the process of growing the field oxide regions **50, 120, 220, 320 and 322** to drive in the boron implanted regions **208** and **308**, or vice versa (See, Kosiak at column 5, lines 32-42).

> FIGS. **3A–3D** are side views in section taken along the line **3—3** of FIG. **2** and illustrate steps in fabricating the device of FIG. **2**. Initially, as shown in FIG. **3A** a P+ substrate **40** and P– epitaxial layer **42** are provided as starting material. Alternatively, the substrate and epitaxial layers can be different conductivity types. A deep P+ Sinker Mask and Implant (Boron at 5E15 dose) is performed for source grounding. For a P– or P+ substrate an N– drift region **46** is formed (Arsenic, 5E10–5E12 dose). A thin oxide growth (150 to 1,500 Å) **48** followed by silicon nitride deposition (0.05 to 0.2 micron) **50** are formed. An active area mask is formed by etching the nitride where the field oxide **52** will be present. The doped sinker region **44** is driven in at 1,000°–1,270° C. for 60–800 minutes and the field oxide **52** is grown to a thickness of 0.5 to 3 microns.

As this is a vertical bipolar transistor, the lightly doped n-type wells **114, 214**, which contain the boron implanted regions **208** and **308**, must be formed prior to the boron implanted regions **208** and **308** themselves. Accordingly, it is very important to the process of Kosiak that its field oxide regions **50, 120, 220, 320** and **322** be formed after implantation of its boron implanted regions **208** and **308,** so as to drive them into the substrate, and further that the boron implanted regions **208** and **308** ultimately need be formed after implantation of its lightly doped n-type wells **114, 214**. Accordingly, Kosiak actually teaches away from forming its field oxide regions **50, 120, 220, 320** and **322** prior to its boron implanted regions **208** and **308** and lightly doped n-type wells **114, 214**. Such a teaching away makes the modification suggested by the Examiner non-obvious, and

thus merely based upon hindsight. The Board of Appeals is well aware that using hindsight, such as is the case here, is impermissible.

Therefore, Kosiak fails to teach or suggest the invention recited in independent Claim 1 and its dependent claims, when considered as a whole. Kosiak must therefore fail to establish a prima facie case of obviousness with respect to these Claims. It is therefore respectfully submitted that claims 1-3 and 21 are not obvious in view of Kosiak.

In view of the foregoing remarks, the cited reference does not support the Examiner's rejection of Claims 1-3 and 21 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests that the Board of Appeals remove the rejection of independent Claim 1 and the Claims dependent thereon.

For the reasons set forth above, the Claims on appeal are not properly rejected under section 35 U.S.C. §§103. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellant's pending claims.

Respectfully submitted,

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Dated: April 21, 2010

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VIII. APPENDIX A - CLAIMS

1. (Previously Presented) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

forming first and second isolation structures within a substrate;

forming a lightly-doped source/drain region between the first and second isolation structures with only a first dopant and without the use of a mask layer between the first and second isolation structures; and

creating a gate over the lightly-doped source/drain region.

2. (Original) The method as recited in Claim 1 wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant.

3. (Original) The method as recited in Claim 2 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm^2 to about 1E13 atoms/cm^2.

Claim 4 (Canceled)

5. (Original) The method as recited in Claim 1 further including diffusing a second dopant at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.

6. (Previously Presented) The method as recited in Claim 5 wherein diffusing the

second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2.

7. (Previously Presented) The method as recited in Claim 5 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant.

8. (Original) The method as recited in Claim 5 further including placing a heavy concentration of the first dopant in a region adjacent a source side of the gate, and in the lightly-doped source/drain region adjacent a drain side of the gate.

9. (Original) The method as recited in Claim 8 wherein placing includes placing the heavy concentration of the first dopant in the lightly-doped source/drain region a distance ranging from about 2000 nm to about 3000 nm from the drain side of the gate.

Claim 10 (Canceled)

11. (Withdrawn) A method of manufacturing an integrated circuit, comprising:

fabricating laterally diffused metal oxide semiconductor (LDMOS) transistors, including:

forming first and second isolation structures in a substrate;

forming a lightly-doped source/drain region between the first and second isolations structures and with only a first dopant; and

creating a gate over the lightly-doped source/drain region;

depositing interlevel dielectric layers over the LDMOS transistors; and

creating interconnect structures in the interlevel dielectric layers and interconnecting the LDMOS transistors to form an operative-integrated circuit.

12. (Withdrawn) The method as recited in Claim 11 wherein forming includes forming a lightly-doped source/drain region with a first N-type dopant.

13. (Withdrawn) The method as recited in Claim 12 wherein the first N-type dopant has an implant dose ranging from about 1E12 atoms/cm^2 to about 1E13 atoms/cm^2.

Claim 14 (Canceled)

15. (Withdrawn) The method as recited in Claim 11 further including diffusing a second dopant at least partially across the lightly-doped source/drain region and under the gate to form a first portion of a channel.

16. (Withdrawn) The method as recited in Claim 15 wherein diffusing the second dopant includes diffusing a P-type dopant having an implant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2.

17. (Withdrawn) The method as recited in Claim 15 wherein diffusing the second

dopant includes diffusing a P-type dopant having an implant dose about 100 times higher than an implant dose of the first dopant.

18. (Withdrawn) The method as recited in Claim 15 further including placing a heavy concentration of the first dopant in a region adjacent a source side of the gate, and in the lightly-doped source/drain region adjacent a drain side of the gate.

Claim 19 (Canceled)

20. (Withdrawn) The method as recited in Claim 18 wherein placing includes placing an implant dose of the first dopant ranging from about 1E15 atoms/cm^2 to about 1E16 atoms/cm^2.

21. (Previously Presented) The method as recited in Claim 1 wherein forming the lightly-doped source/drain region includes forming the lightly-doped source/drain region using a blanket implant process over the entire substrate.

22. (Withdrawn) The method as recited in Claim 11 wherein forming the lightly-doped source/drain region includes forming the lightly-doped source/drain region using a blanket implant process over the entire substrate.

23. (Withdrawn) A method of manufacturing a laterally diffused metal oxide semiconductor (LDMOS) device, comprising:

forming first and second isolation structures within a substrate, the first isolation structure having a first edge and a second edge and the second isolation structure having a third edge and a fourth edge;

forming a lightly-doped source/drain region between the first and second isolation structures with only a first dopant, the lightly-doped source/drain region in contact with the second edge of the first isolation structure and the third edge of the second isolation structure; and

creating a gate over the lightly-doped source/drain region and between the first and second isolation structures.

24. (Withdrawn) The method as recited in Claim 23 wherein the first and second isolation structures are first and second field oxide isolation structures.

IX. APPENDIX B - EVIDENCE

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE